AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-28. (Canceled)

29. (Currently Amended) A semiconductor device comprising:

a substrate; ~~having~~

a first gate electrode formed at an upper portion of the substrate;[[,]]

a source and a drain formed in the substrate at ~~a lower portion of~~ both sides of ~~said~~ the first gate electrode;

an etch stop layer formed on the substrate, including on the first gate electrode;

an undoped insulating layer ~~interposed~~ formed on the etch stop layer; and

~~an~~ a doped insulating layer ~~continuously~~ formed on the substrate, the etch stop layer, the undoped insulating layer, and the first gate electrode~~, the insulating layer being formed by (a) flowing the oxidizing gas at the oxidizing gas flow rate, (b) flowing the first carrier gas at the first carrier gas flow rate while carrying a first impurity including boron flowing at a first impurity flow rate, (c) flowing the second carrier gas at the second carrier gas flow rate while carrying a second impurity including phosphorus flowing at a second impurity flow rate, and (d) flowing a silicon source material at a silicon source flow rate,~~

wherein, for the doped insulating layer composition, a ratio of ~~the~~ an oxidizing gas flow rate, ~~the~~ a first carrier gas flow rate, ~~the~~ a second carrier gas flow rate, ~~the~~ a silicon source flow rate, ~~the~~ a first impurity flow rate, and ~~the~~ a second impurity flow rate is about 2.00 - 2.50 : 0.70 - 0.95 : 1 : 0.15 - 0.25 : 0.040 - 0.045 : 0.013 - 0.014, and wherein a flow rate of ~~the~~ a second carrier gas is at least 4,000 sccm.

30-33. (Cancelled)

34. (Previously Presented) The semiconductor device as claimed in claim 29, wherein a thickness of the etch stop layer is about 60-150 Å.

35. (Currently Amended) The semiconductor device as claimed in claim 29, wherein the doped insulating layer is a borophosphosilicate glass layer.

36. (Currently Amended) ~~The semiconductor device as claimed in claim 29,~~ A semiconductor device comprising:

a substrate;

a first gate electrode disposed on an upper portion of the substrate;

a source and a drain disposed in the substrate at both sides of the first gate electrode;

an etch stop layer disposed on the substrate including the first gate electrode;

an undoped insulating layer disposed on the etch stop layer; and

a doped insulating layer disposed on the substrate, the etch stop layer, the undoped insulating layer, and the first gate electrode,

wherein the doped insulating layer contains about 5.5% by weight of boron and about 3.0% by weight of phosphorus.

37. (Currently Amended) The semiconductor device as claimed in claim 29, wherein a thickness of the doped insulating layer is about 9,500 Å.

38. (New) The semiconductor device as claimed in claim 29, further comprising:

a second gate electrode formed at an upper portion of the substrate laterally spaced apart from the first gate electrode,

wherein the etch stop layer, the undoped insulating layer, and the doped insulating layer are all formed on the second gate electrode,

wherein the doped insulating layer has a hole formed therein between the first and the second gate electrodes, and

wherein sidewalls of the hole comprise the doped insulating layer such that the hole is separated and spaced apart from the first and the second gate electrodes.

39. (New) The semiconductor device as claimed in claim 36, further comprising:

a second gate electrode formed at an upper portion of the substrate laterally spaced apart from the first gate electrode,

wherein the doped insulating layer has a hole formed therein between the first and the second gate electrodes, and

wherein sidewalls of the hole comprise the doped insulating layer such that the hole is separated and spaced apart from the first and the second gate electrodes.